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10/596,693	01/30/2007	**Bini Elhanan**	06727/0205059-US0	9541

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DARBY & DARBY P.C.
P.O. BOX 770
Church Street Station
New York, NY 10008-0770

EXAMINER	
BAHTA, KIDEST	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/596,693	ELHANAN ET AL.	
	Examiner	Art Unit	
	KIDEST BAHTA	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59 and 88-130* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27,53-55,59,88-119,121-123,125-128 and 130* is/are rejected.

7)☒ Claim(s) *28-52,56-58,120,124 and 129* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 3/16/10 has been received and fully considered; claims 1-59 and 88-130 are presented for examination. Claims 60-87 and 131-149 are cancelled.

2. Regarding to objection claims, the Examiner withdraws the rejections since applicant amend the claims.

3. Regarding the rejection under double patenting, the Examiner maintains the rejections as Applicant fail to overcome the rejection; Applicant didn't file the terminal disclaimer.

Response to Arguments

4. Applicant's amendments filed 3/16/10 have been fully considered, but they are not persuasive.

Applicant argues that Kou does not show or suggest the method of manufacturing electronic circuits of the present invention, as recited in amended claims 1 and 88 including, inter alia, automatically generating pick & place machine-specific component data by employing a first database containing pick & place machine-independent, geometric component data and a second database containing machine-specific, component manufacturer-independent rules for generating the pick & place machine-specific component data. However examiner disagrees since Kou disclose such limitation in Fig. 3, 5, 15 and column 7, lines 8-19; column 10, lines 55-62; i.e., A key reader may be provided at the scanning station to automatically read the feeder

identification code when the operator scans the part number, or the key identification code can be duplicated on a scannable bar code attached to the feeder.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-59 and 88-130 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 60-87 and 131-149 of U.S. Patent No. 7,599,757, 7,447,560 and 7,440,813, respectively. Although the conflicting claims are not identical, they are not patentably distinct from each other because the limitation of the claims are same subject matter as a pick and place machine-specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-27, 53-55, 59, 88-119, 121-123, 126-128 and 130 are rejected under 35 U.S.C. 102(b) as being anticipated by Kou et al. (US 6,778,878).

Regarding claims 1-27, 53-55 and 59 Kou discloses:

1. A method of manufacturing electronic circuits comprising:

generating CAD data, a bill of materials and an approved component vendor list for an electronic circuit (Column 5, 51-61); and

employing said CAD data, said bill of materials and said approved component vendor list for automatically generating :

a pick & place machine-specific component loading specification (Column 5, 51-61);

a pick & place machine-specific component placement sequence(Column 3, 43-59); and

pick & place machine-specific component data for governing the operation of at least one specific pick & place machine in a manufacturing line (column 8, 15-21).

2. A method of manufacturing electronic circuits according to claim 1 and wherein said employing said CAD data, said bill of materials and said approved component vendor

list for automatically generating pick & place machine specific component data for governing the operation of at least one specific pick & place machine includes:

automatically generating said pick & place machine-specific component data by employing a first database containing at least one of pick & place machine-independent, geometric component data and pick & place machine-independent, component supply data and a second database containing machine-specific, component manufacturer-independent rules for generating said pick & place machine-specific component data (Fig. 3, 5, and 15; column 7, lines 8-19).

3. A method of manufacturing electronic circuits according to claim 1 and wherein said pick & place machine specific component data for governing the operation of at least one specific pick & place machine comprises at least one of pick & place machine-specific component shape parameters and pick & place machine-specific component supply parameters (column 7, lines 20-58).

4. A method of manufacturing electronic circuits according to claim 1 and wherein said automatically generating pick & place machine-specific component data comprises automatically generating a third database containing at least:

a mapping between component identifiers and pick & place machine-specific component shape parameters (column 6, 2-25); and

a mapping between said component identifiers and pick & place machine-specific component supply parameters(column 6, 2-25).

5. A method of manufacturing electronic circuits according to claim 4 and wherein said mapping between component identifiers and pick & place machine-specific component shape parameters comprises:

a mapping of PCNs to component shape identifiers(column 6, 2-25); and

a mapping of component shape identifiers to pick & place machine-specific component shape parameters(column 6, 2-25).

6. A method of manufacturing electronic circuits according to claim 5 and wherein said component shape identifiers are pick & place machine-specific component shape identifiers (column 6, 2-25).

7. A method of manufacturing electronic circuits according to claim 4 and wherein said mapping between said component identifiers and pick & place machine-specific component supply parameters comprises:

a mapping of PCNs to component supply identifiers (column 6, 2-25); and

a mapping of component supply identifiers to pick & place machine-specific component supply parameters(column 6, 2-25).

8. A method of manufacturing electronic circuits according to claim 7 and wherein said component supply identifiers are pick & place machine-specific component supply identifiers (Fig.3).

9. A method of manufacturing electronic circuits according to claim 4 and wherein said pick & place machine-specific component shape parameters *include at least one of:*

component geometry parameters;

component handling parameters;

component imaging parameters;

component recognition tolerances; and

pick & place machine-specific procedures (Abstract).

10. A method of manufacturing electronic circuits according to claim 4 and wherein said pick & place machine-specific component shape parameters *include at least one of:*

component geometry parameters in pick & place machine-specific syntax;

pick & place machine-specific component handling parameters;

pick & place machine-specific component imaging parameters;

pick & place machine-specific component recognition tolerances; and

pick & place machine-specific procedures (Fig. 3).

11. A method of manufacturing electronic circuits according to claim 4 and wherein said pick & place machine-specific component supply parameters *include at least one of:*

a component carrier type (Fig. 2); and

pick & place machine-specific, component carrier-specific parameters.

12. A method of manufacturing electronic circuits according to claim 1 and wherein at least part of said pick & place machine-specific component data comprises adaptive pick & place machine-specific component data (Fig. 5).

13. A method of manufacturing electronic circuits according to claim 12 and wherein said adaptive pick & place machine specific component data comprises adaptive pick & place machine specific component shape data (Column 7, lines 20-58).

14. A method of manufacturing electronic circuits according to claim 12 and wherein said adaptive pick & place machine specific component data comprises adaptive pick & place machine specific component supply data (column 7, lines 20-58).

15. A method of manufacturing electronic circuits according to claim 2 and wherein said first database *comprises at least one of:*

a mapping of CV/Cat#s to component vendor-specific component geometric parameters (CCL);

a mapping of CV/Cat#s to component supply form parameters (CCSL);

a mapping of PCNs to component supply form parameters (UMCSL);

a mapping of PCNs to CV/Cat#s (MCVL);a mapping of DCN to PCN;

a user maintained mapping of CV/Cat# to component vendor-specific component geometric parameters (UMCL); and

a mapping of PCN to generic component geometric parameters (column 6, lines 2-25).

16. A method of manufacturing electronic circuits according to claim 2 and wherein said second database *comprises at least one of:*

a mapping of component manufacturer-independent component characteristics to rules for generating pick & place machine-specific component shape parameters; and

a mapping of component manufacturer-independent component supply form characteristics to rules for generating pick & place machine-specific component supply parameters (column 6, lines 2-25).

17. A method of manufacturing electronic circuits according to claim 16 and wherein said rules for generating pick & place machine-specific component shape parameters include rules for *generating at least one of:*

component geometric parameters in pick & place machine specific syntax;

pick & place machine specific component handling parameters;

pick & place machine specific component imaging parameters;

pick & place machine specific component recognition tolerances; and

pick & place machine specific procedures (Fig. 3).

18. A method of manufacturing electronic circuits according to claim 16 and wherein

said rules for generating pick & place machine-specific component supply parameters include rules for *generating at least one of:*

a component carrier type in pick & place machine-specific syntax (Column 3, lines 50-65); and component carrier type-specific parameters in pick & place machine-specific syntax.

19. A method of manufacturing electronic circuits according to claim 16 and wherein said second database comprises *at least one of*:

a mapping of component manufacturer-independent component characteristics to rules for generating adaptive pick & place machine-specific component shape parameters; and

a mapping of component manufacturer-independent component supply form characteristics to rules for generating adaptive pick & place machine-specific component supply parameters (Fig. 3-5).

20. A method of manufacturing electronic circuits according to claim 19 and wherein said rules for generating adaptive pick & place machine-specific component shape parameters include rules for *generating at least one of:*

component geometric parameters in pick & place machine specific syntax;

adaptive pick & place machine specific component handling parameters;

adaptive pick & place machine specific component imaging parameters;

adaptive pick & place machine specific component recognition tolerances; and pick & place machine specific procedures (Fig. 3).

21. A method of manufacturing electronic circuits according to claim 19 and wherein said rules for generating adaptive pick & place machine-specific component supply parameters include rules for *generating at least one of:*

adaptive component carrier type in pick & place machine-specific syntax; and adaptive component carrier type-specific parameters in pick & place machine-specific syntax (column 6, lines 2-25).

22. A method of manufacturing electronic circuits according to claim 1 and wherein said second database is operator modifiable.

23. A method of manufacturing electronic circuits according to claim 1 and wherein said employing said CAD data, said bill of materials and said approved component vendor list for automatically generating pick & place machine specific component data for governing the operation of at least one specific pick & place machine includes: automatically generating said pick & place machine-specific component data by employing a fourth database containing pick & place line and machine configurations.

24. A method of manufacturing electronic circuits according to claim 23 and wherein said fourth database *comprises at least one of*:

pick & place machine configurations;

ordered listings of pick & place machines in at least one machine line (column 3, lines 43-57); and

pick & place machine configurations of said pick & place machines in said at least one machine line.

25. A method of manufacturing electronic circuits according to claim 24 and wherein said pick & place machine configurations *include at least one of*:

camera types and characteristics;

illumination types and characteristics;

component feeder carriage types and characteristics (column 5, lines 36-51);

component feeder types and characteristics;

nozzle types and characteristics; and

kinetic characteristics of moving elements (Fig. 15).

26. A method of manufacturing electronic circuits according to claim 24 and wherein said pick & place machine configurations of said pick & place machines in said plurality of machine *lines include at least one of:*

mounted camera types;

mounted illumination types;

mounted component feeder carriages (column 5, lines 36-51);

mounted component feeders (element 16); and

mounted nozzles.

27. A method of manufacturing electronic circuits according to claim 2 and wherein said employing said CAD data, said bill of materials and said approved component vendor list for automatically generating pick & place machine-specific component loading specification, pick & place machine-specific component placement sequence and pick & place machine-specific component data for governing the operation of at least one specific pick & place machine in a manufacturing line comprises:

employing said CAD data, said bill of materials, said approved component vendor list and said first database to search for component data for new components (Fig. 1); and employing said first database and said second database to auto-generate said pick & place machine specific component data (Fig. 5, column 7, lines 40-49).

52. A method of manufacturing electronic circuits according to claim 51 and also comprising, prior to said employing at least part of said GCG parameters to access appropriate ones of said machine-specific, component manufacturer-independent rules, employing at least part of said GCG parameters to auto-generate said corresponding pick & place machine specific component shape identifier (column 8, lines 9-46).

53. A method of manufacturing electronic circuits according to claim 27 and also comprising, prior to said employing said CAD data, said bill of materials, said approved component vendor list and said first database, automatically populating a CCL portion of

said first database (Fig. 10; column 9, lines 7-36).

54. A method of manufacturing electronic circuits according to claim 53 and wherein said automatically populating comprises employing a component library which maps CV/CAT#s to component packaging shape parameters ((column 11, lines 35-54; Fig. 15).

55. A method of manufacturing electronic circuits according to claim 54 and wherein said employing a component library comprises employing said component library which includes:

a first stage mapping which maps CV/CAT#s to component packaging shape identifiers Fig. 15); and

a second stage mapping which maps said component packaging shape identifiers to component packaging shape parameters (Fig. 15).

As claims 88-119, 121-123, 126-128 and 130 the same rejection applies as claims 1-27, 53-55, and 59.

Allowable Subject Matter

7. Claims 28-52, 56-58, 120, 124-125 and 129 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form

including all of the limitations of the base claim and any intervening claims and by filing terminal disclaimers to overcome the rejections of Double Patenting.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed Kidest Bahta whose telephone number is 571-272-3737.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application information Retrieval lPAIRI system. Status information for published applications may be obtained from either Private PMR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-fee).

/Kidest Bahta/

Primary Examiner, Art Unit 2125